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ABSTRACT

This report describes an investigation of a technique for producing paper copies of instructional computer terminal displays. Such a device appears to be a useful adjunct for the development of computer-assisted instructional programs by authors. A digital device was simulated with a minicomputer; the techniques used to construct this device are described inthis technical report. Examples of the hard copy produced and a description of the computer program used in the simulation are included in this report. (Author)

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DEVELOPMENT OF A PLASMA PANEL HARD COPY UNIT

By

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December 1975
Final Report for Period February 1975 – November 1975

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MARTY R. ROCKWAY, Technical Director
Technical Training Division

Approved for publication.

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Commander

SUMMARY

Problem

The plasma display interactive computer terminal used in the Air Force Advanced Instructional System computer network provided no facility for the production of printed copy of display images. This prevented the programmer/author from capturing information created during program development for analysis and debugging. Proposed hard copy units under commercial development appeared to be too costly and unreliable for volume use within the training environment. The purpose of this work unit was to investigate an alternative approach to the hard copy problem and to obtain an in-house unit for use if the approach proved successful.

Approach

The desired approach was to develop a special random access digital memory using the same dot addressing scheme as the plasma display panel. The memory would function as a digital dot map of the 512 by 512 array of dots presented visually by the plasma panel. The contents of this memory could thus be printed on demand on a dot line printer. Since the construction of this memory would be rather time consuming, it was decided that the memory would be simulated on an available PDP-11 minicomputer. A simple interface from the plasma display connector to the PDP-11 was built to allow the PDP-11 to monitor write and erase requests to the plasma panel. A program to enable the PDP-11 to print the contents of the simulated memory on a Versatec dot printer resides in the minicomputer while the hard copy process is active.

Results

The digital approach to making hard copy worked as anticipated and is feasible for use in volume in the training environment. The dot printer used in this device appears to be highly reliable and produces high quality, high contrast copies. The production of actual hardware for the dot memory would be possible with in-house resources if no acceptable commercial alternative becomes available.

Conclusions

The development of the in-house capability to make hard copy has proven quite beneficial for software development and represents a feasible alternative for future hard copy devices for use in the authoring environment.

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DEVELOPMENT OF A PLASMA PANEL HARD COPY UNIT

I. INTRODUCTION

The Air Force Human Resources Laboratory, Technical Training Division (AFHRL-TT), Lowry Air Force Base, Colorado, is responsible for the development of the Advanced Instructional System (AIS). The AIS includes a large computer system to prescribe instructional resources and present on-line instruction at interactive graphic computer terminals. The terminal used in this system is built around a plasma discharge screen which displays computer generated graphics and characters in an array of 512 by 512 dots. This array appears to the user as glowing orange dots on a black background, in an approximately 8.5 by 8.5 inch square. Each dot can be individually set or reset and will remember its state until further altered. In addition the entire screen may be erased in a single operation.

Although there are many advantages to developing software at such a terminal, a significant disadvantage is that graphic images, and often interactively built up character groupings, cannot be printed on a system line printer for program debugging and analysis. This causes problems during instructional materials authoring since the results of a debugging session disappear as a program is run, leaving the author nothing to work with but notes and memories.

This work unit was established to obtain an in-house capability to produce hard copy, and to investigate an all digital approach to the construction of such a unit. Several constraining factors were the limited manpower to support hardware development, and a strong desire to obtain the hard copy capability as soon as possible. Consequently, the approach undertaken minimized hardware design and reduced effort to approximately four man-weeks. The resulting device has been in use for many months and has proven the feasibility of the technique and the reliability of a digital rather than optical approach to this problem.

II. THEORY OF OPERATION

Plasma Panel

The plasma panel can be considered to be a square array of illuminable dots each of which remembers whether it is illuminated. Each dot is directly addressible by specification of 1 of 512 possible rows, and of 1 of 512 columns located within this row. Unlike in typical digital memories, bits (dots) are not grouped together in words but are rather handled as single dots at all times. The electrical interface to the panel designates both row and column addresses to the panel as 9 bit binary numbers using 18 parallel, active high, standard TTL logic signals. A request to change a particular dot always consists of these 18 levels and either of two possible strobe signals. The strobe signals are also active high standard TTL logic levels.

The physical design of the plasma display is based on two flat plates of glass held precisely apart forming a chamber which is filled with gas. Just below the interior surface of each plate is a grid of electrical conductors, horizontally placed in the front sheet and vertically placed in the rear sheet. These conductors are electrically insulated from the gas mixture by a very thin glass coating. The entire front grid of conductors is made to change polarity with respect to the back grid at a rate of 50 Kilohertz with a potential of about 170 volts. The result of this alternating field is that if a charge is placed at the intersection of any two grids on one surface of the glass it will jump back and forth between the glass surfaces ionizing the neon gas at the intersection and causing a characteristic neon orange glow. By careful control of the resistivity of the insulating glass each discharge is effectively isolated from other discharges even though they are less than 1/60th of an inch apart. The rate at which the grid potentials must be reversed is critically related to the gas mixture, pressure, and other variables and is also a determinant of the rate at which dots in the display may be written.

Because a dot may only be changed at a certain point in the refresh cycle, the refresh rate of 50 kHz produces an allowable write frequency of 1/50000 of a second, or 20 microseconds/bit. This cycle is fully synchronous independent of any writing requests, so requests from the plasma terminal hardware to write on the panel must be synchronized to the panel refresh cycle. This is ensured by a TTL "busy" signal generated by the plasma panel. This signal goes "not ready" when a write or bulk erase signal is issued to the panel, and returns to the ready state when the panel is synchronously ready to accept further data. The effect of this characteristic on a hard copy unit is that the hard copy unit must be capable of recording data

sent to the panel in the time taken by the panel refresh cycle. No delay may be added by the hard copy circuitry without disturbing the synchronous cycle of the panel.

Hard Copy Unit

The hard copy unit to be described in this report is a simulation of a hardware device which has not been built. The simulation exhibits most of the behavior of the actual device, and produces the same hard copy. The simulation consists of a PDP-11 minicomputer replacing a hardware digital memory, a Versatec 200 dot plotter, and a simple interface box connecting a plasma panel to the PDP-11. The simulation can do everything a hardware unit could do except rapid full screen erase. In order to understand how the simulation works, it is first necessary to understand how a hardware version would operate.

A hardware version of this device would be built as a 512 by 512 by 1 bit digital memory. The two nine bit addresses (used to address the plasma panel) would select a particular bit in the digital memory. This bit would be either set or reset corresponding to whether the associated bit in the panel was illuminated or dark. Special circuitry would be included to allow all chips in the memory to be erased simultaneously to ensure a rapid erasure of memory contents analogous to the bulk erasure capability of the plasma panel. This memory would also be addressible by a built in microprocessor which would allow the contents to be moved to any of several possible types of dot printers, and to allow for special effects such as continued (from screen to screen) plots or inverted (white on black) images. Such a device is certainly well within current technology, and the cost of building it drops with each improvement in random access memory technology. With current costs it should be achievable with less than $1,000.00 in components.

The simulated hard copy unit works analogously to the actual hardware hard copy unit. The primary difference is that rather than building a hardware memory array, a 16,384 word portion of the address space of a PDP-11 minicomputer is used to store dot array images. The microprocessor is replaced by the minicomputer processor which can of course address the built in 16,384 words of core memory. Storage into the memory is performed under program control through input/output ports. The program which controls mapping into the dot memory resides in additional storage space and is normally loaded into core from disk unless it is already resident when copying is to begin.

A typical copying session begins with the loading of the hard copy program into the PDP-11. The copy program clears the 16,384 word memory, simulating a full screen erase of the plasma display, and begins a tight monitoring loop watching write requests issued to the plasma display by the computer terminal which houses the display. When the minicomputer detects a write request, it copies the plasma screen address into one of its registers and uses this address as an index into the 16,384 word dot array. It moves the contents of the selected word to an output port where the selected bit is altered by a hardware multiplexor, external to the PDP-11, using the write and erase request lines to set or reset the selected bit. The patched word is then moved through an input port back into the dot array, and the monitoring loop is repeated.

This monitoring loop continues until stopped by the person operating the copier. The operator halts the minicomputer and starts it again at the address of a program which prints the contents of the internal memory on the Versatec dot printer. At this time, the operator may press a continue switch for additional copies of the same image, or may restart the process by clearing the PDP-11 dot memory. A single copy takes about 15 seconds considering operator steps, and additional copies take about 10 seconds each.

III. DETAILED DISCUSSION

Terminal Control of the Plasma Panel

The plasma terminal issues all requests to the plasma display panel through 21 active high TTL data signals. Eighteen of these signals are levels used as two nine bit addresses for row and column as explained above. Two strobe signals of ~ 2 microseconds duration are sent at the same time as the address signals. Only one of these signals is ever active for a given request, one signaling a request to illuminate the addressed dot, and the other signaling a request to erase the addressed dot. An additional signal is available requesting a bulk erasure but this is not implemented since the PDP-11 could not perform this operation at

the execution speed of the plasma panel, and would thus lose data issued immediately after the bulk erase request. An illustration of I/O logic for the modified system is included in Figure 1.

The dot array of the panel is mapped as an array of rows in the PDP-11 memory. Each horizontal line on the panel is treated as a group of 32 PDP-11 words. The lower four bits of the panel X axis address is used by a hardware multiplexor board to select a particular bit in a display row. The other five bits of X address are used as the five least significant bits of address within the 16,384 word PDP-11 array. The nine bits of the Y axis panel address are used as the most significant bits of the array address. Thus, 14 lines must be interfaced to the PDP-11, and used as an internal address into the dot matrix. The remaining four bits never enter the computer but do control the multiplexor. This mapping is depicted in Figure 2.

The terminal begins synchronous operation with the plasma panel by strobing either the write or erase strobes of the plasma panel. The panel waits until an appropriate point in the refresh cycle and then responds to this initial request. The terminal is constructed so that it will have created the next request while the initial request is processed by the panel. The panel signals completion of the original request by its ready line, and since an additional request is waiting, will process that request immediately. If the additional request were not ready at this time, the panel would not be able to accept it until the 20 microsecond refresh cycle had been performed. Since the panel might have to draw as many as 512 dots (one full length screen vector) within 16.6 milliseconds (due to basic data receipt rates not discussed here), each cycle must be used. This can be easily seen since 512 x 20 microseconds = 10.240 milliseconds and could not be doubled since 512 x 40 = 20.480 milliseconds is longer than the real time available to produce the required vector. Thus, the ability of a hard copy device to work in harmony with this system depends upon a rapid bit copy cycle always shorter than 20 microseconds.

The Multiplexor Board

A critical part of the hard copy unit is a simple multiplexing device. This device is used to replace actual bits in a selected word of dot memory with set or reset bits depending upon the request issued to the plasma panel. This bit masking and insert process is typically done by software in a device such as this, but could not be done this way due to the time which would be required to perform this process in software.

The design of this board is that of a 16 element array of 2 to 1 multiplexors. At any time, fifteen of these multiplexors will be selecting as their output fifteen data lines coming from a PDP-11 output port. The remaining multiplexor will be relaying the value of a flip-flop in the controller board which will be set if a panel write request is being processed and reset if a panel erase is being processed. The multiplexor relaying set-reset data is chosen by a 4 to 16 line decoder chip (IC18) also located on the multiplexor board. The four lines used to control the multiplexor are simply the least significant bits of the column address.

The physical layout of this board is such that it plugs into both an output and input port of the PDP-11 minicomputer and efficiently receives a full 16-bit word from the dot array, and returns the modified result into the adjacent port, thus eliminating connectors and cables for this data. This physical relationship may be seen in Figure 3.

Each of the individual 2 to 1 multiplexors was built from a single SN7400 quad NAND gate and is composed of IC1..IC16 on the B2 multiplexor board. A typical circuit for each multiplexor is included in Figure 4. IC17 is simply a buffer for the Write/Erase (W/E) line which amplifies the signal to drive the 16 multiplexors. A wiring diagram of the B2 multiplexor board is presented in Figure 5.

Control Board–B1

The control board for the hard copier interfaces the terminal/plasma panel signals to the multiplexor and PDP-11. The WRITE and ERASE signals from the panel are gated together such that either signal triggers a 1-shot multivibrator (IC21) which in turn triggers another 1-shot which creates the ~ microsecond READY-A signal which is being software monitored by the PDP-11. The first 1-shot also latches the the write/erase signal into a flip-flop (IC22) on this board. The latched signal constitutes the W/E signal which is used to set or reset a bit in the dot array when the multiplexor board is activated by software.

Timing on this board is not critical, however the duration of the READY-A signal must be long enough to be seen by the software monitoring loop, but short enough so that it has vanished by the time

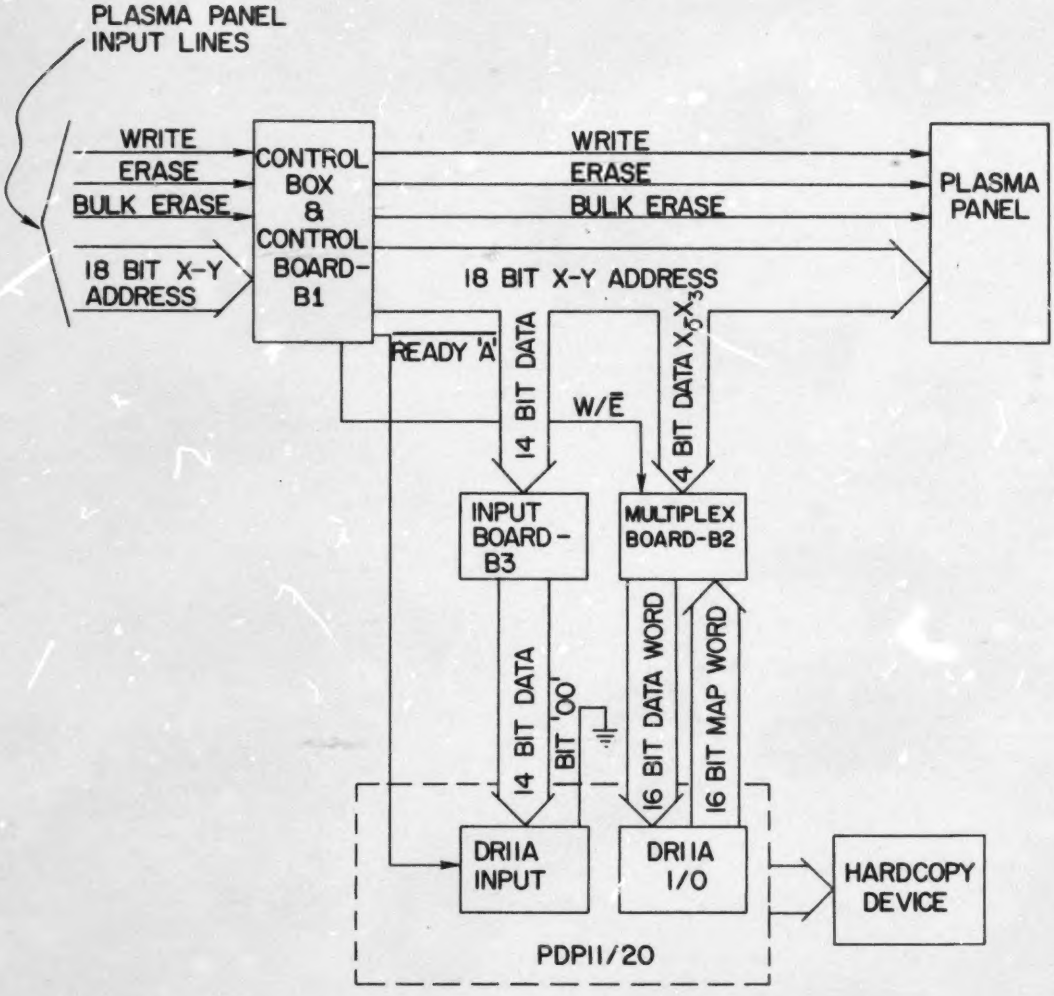
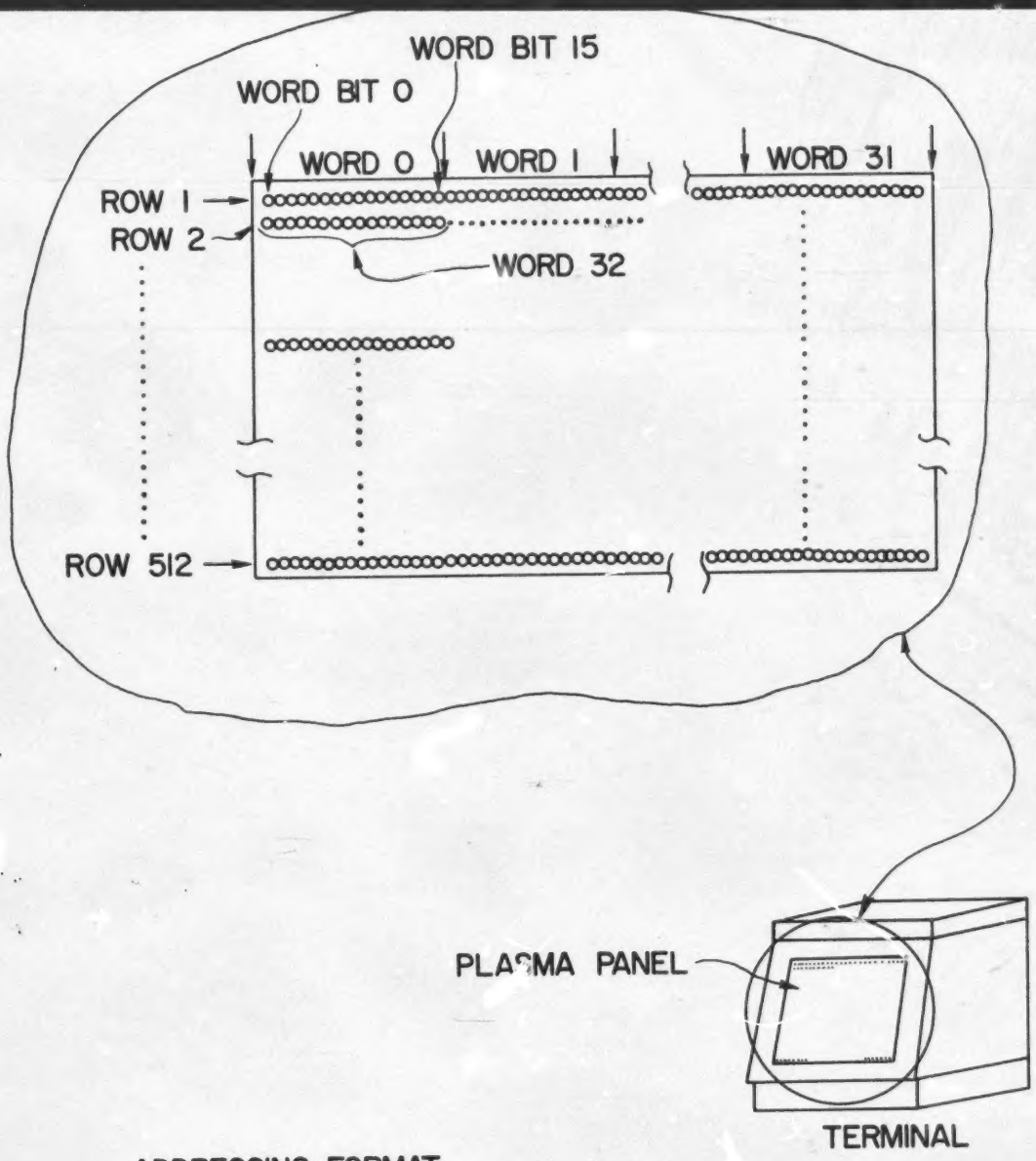


Figure 1. **I/O Bus circuitry block diagram**



ADDRESSING FORMAT

FIRST NINE BITS DETERMINE ONE OF 512 ROWS.
NEXT FIVE BITS DETERMINE ONE OF 32 WORDS/ROW.
LAST FOUR BITS SELECTS ONE OF 16 BITS/WORD THAT WILL EITHER BE TURNED ON OR OFF BY W/$\bar{E}$.

Figure 2. **Pictorial addressing map.**

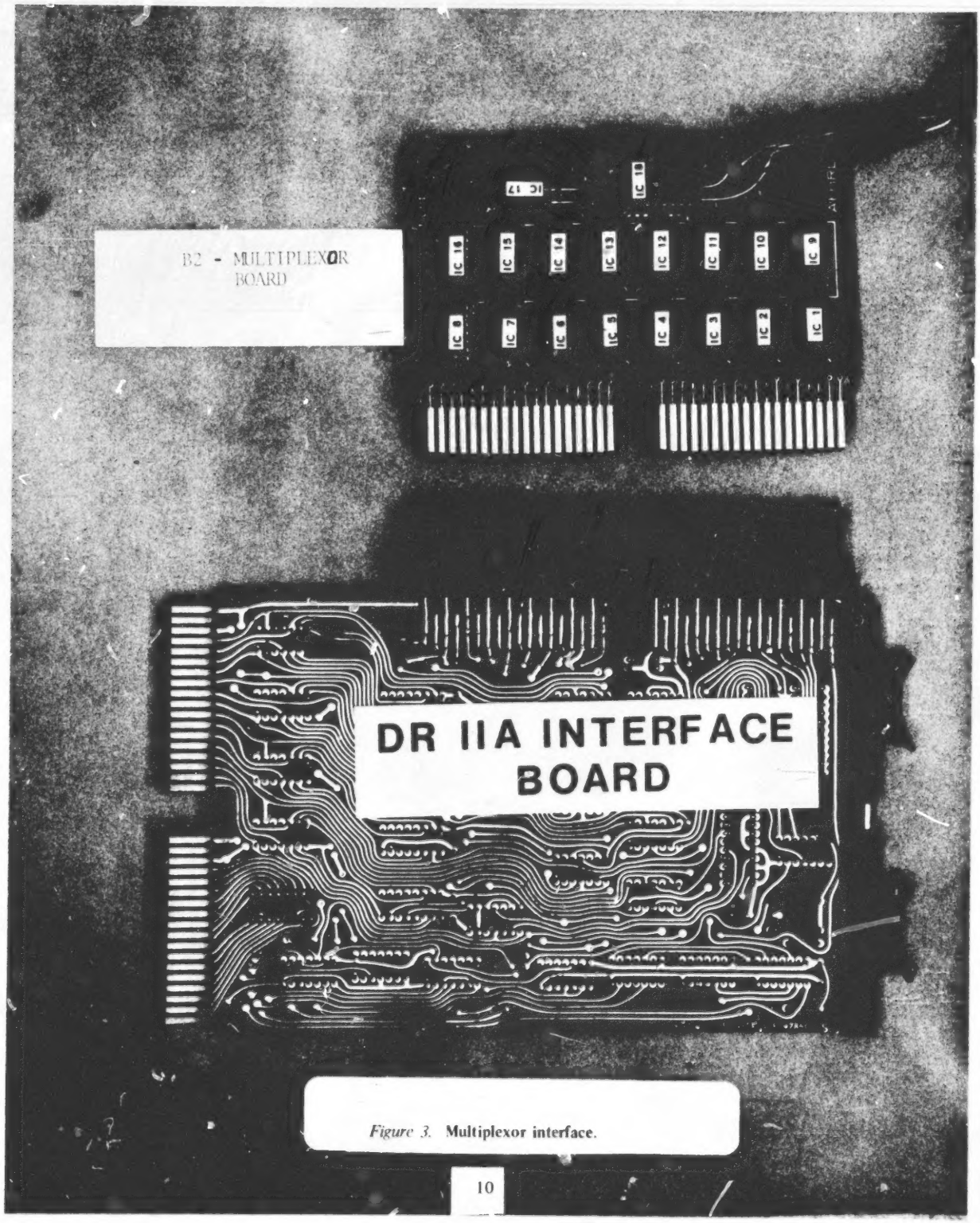
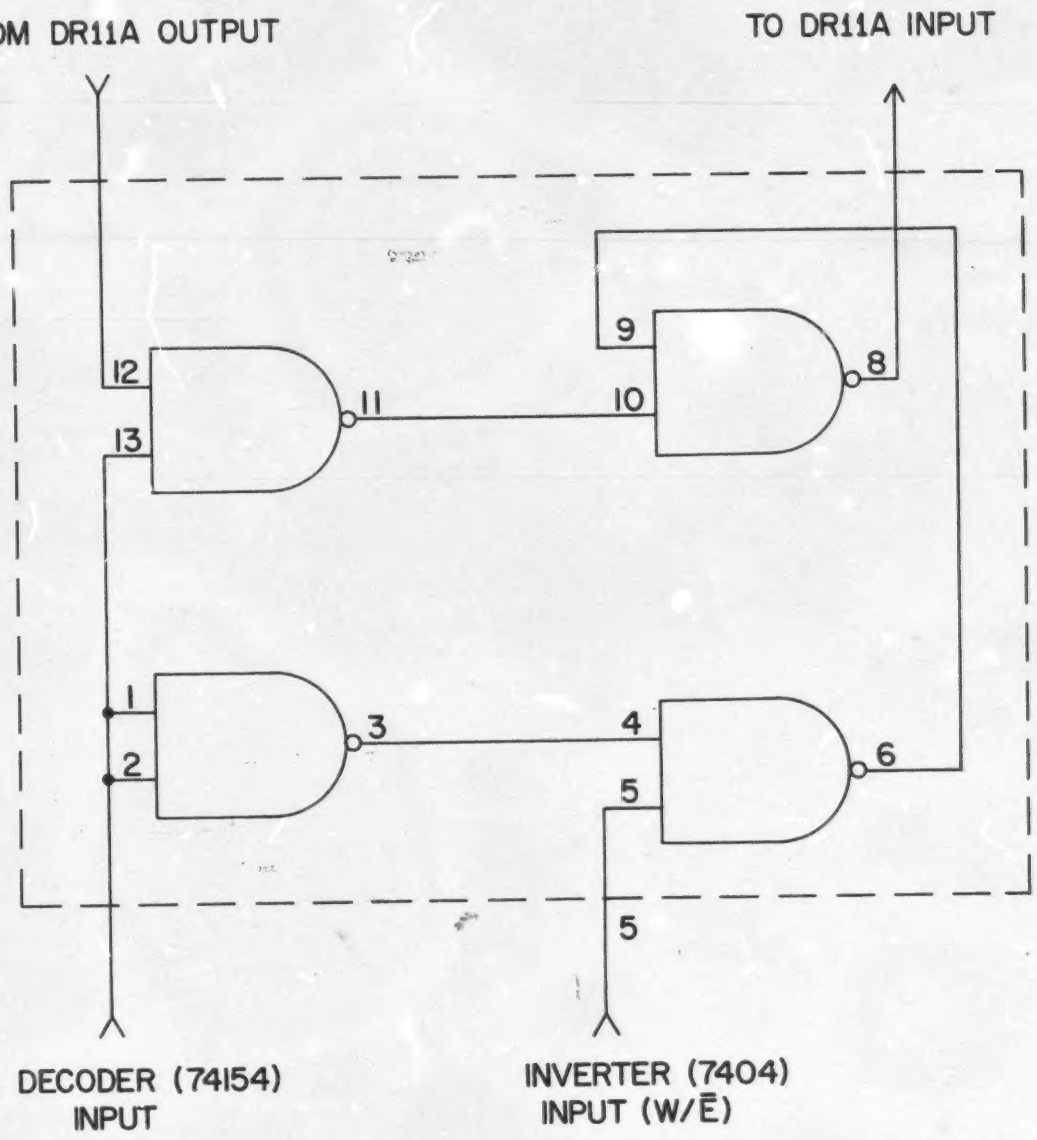


Figure 3. **Multiplexor interface.**



NOTE
DECODER INPUT
DR11A INPUT AND
OUTPUT ARE HARD
WIRED ON BOARD B2

Figure 4. **Typical B2 multiplexor circuit.**

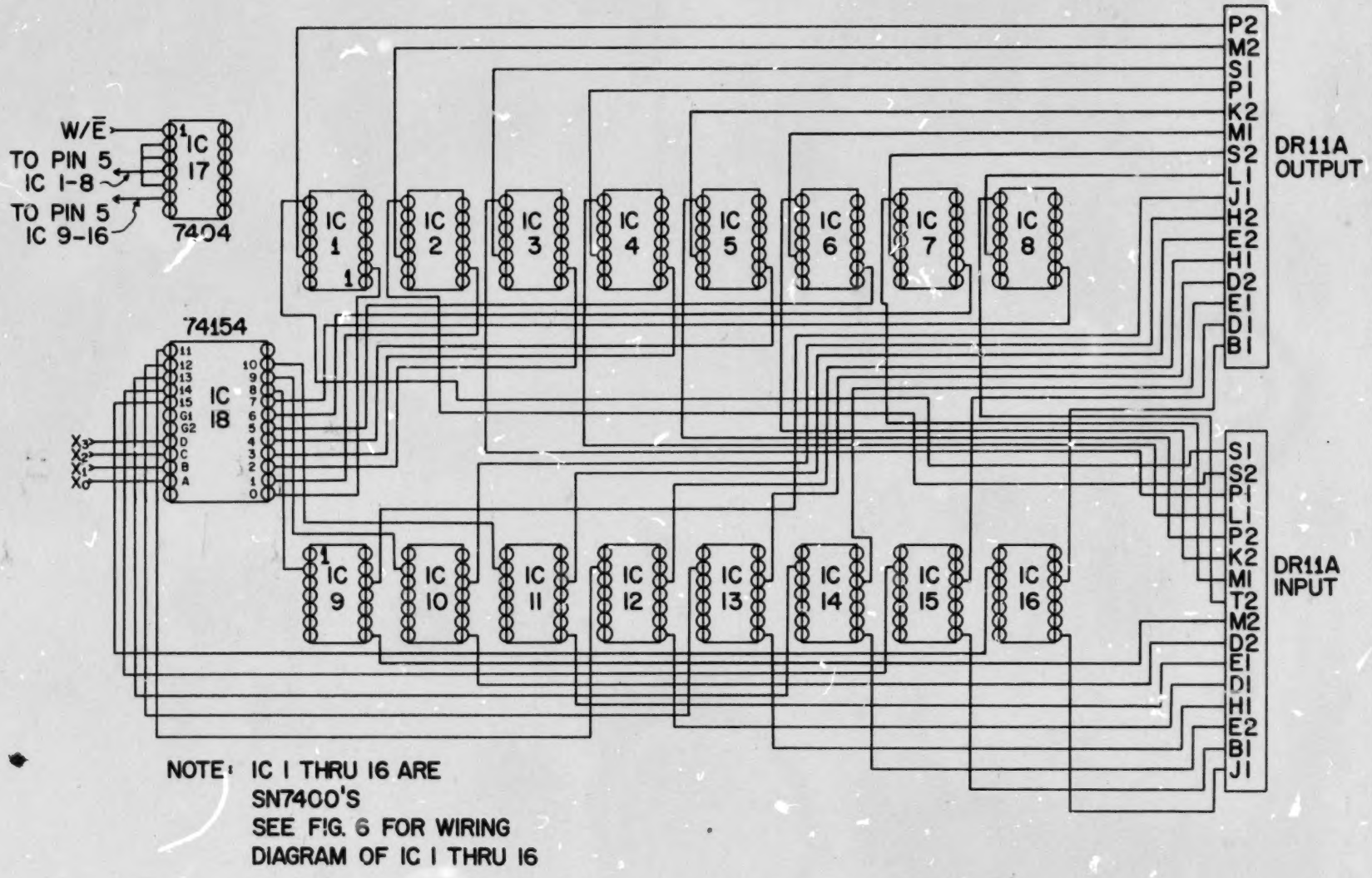


Figure 5. **Multiplexor board—B2-wiring diagram.**

that the requested patching has finished, or a false request will be generated. R2 has been set for ∿ 2 microseconds for the first 1-shot and ∿ 10 microseconds for the second. The RC network attached to the flip-flop generates a clear signal for this flop when power is first applied to the circuit. A schematic of this board is shown in Figure 6 and the interconnection diagram is included in Figure 7.

Input Board– B3

The fourteen most significant address lines from the plasma panel address are used to select one of 16,384 words from the PDP-11 memory. These lines and the READY A line from the control board B2 are routed to input board B3. This board plugs into a PDP-11 input port and is read into the monitoring loop as a single word of data. The READY A line is fed into the sign bit position of the PDP-11 port. When the active low READY A line goes low (i.e., logical zero) it is detected as a sign change in the monitoring loop. The fourteen address lines are fed into bits 1...14 in the PDP-11, and thus appear as a normal PDP-11 word address when the sign bit drops to zero. Bit 0 is always held at zero, which is necessary since it constitutes a half-word (byte) address when it is non-zero. Thus the word address to be changed and the change request flag (READY A) enter the PDP-11 at the same time and with only one instruction execution. Such speed ploys are absolutely essential for the monitoring loop to work correctly.

The PDP-11 Monitoring Software

The program which operates the hard copy simulation resides in PDP-11 address space just above the 16,384 word dot array. This program consists of three major sections: initialization, monitoring loop, and printout loop. The program is written in PDP-11 assembly language and can be loaded into memory using standard PDP-11 Disk Operating System software. Once the program is loaded and starts, it destroys the operating system to use the low address PDP-11 memory to contain its dot array, since interrupt vectors for the PDP-11 normally lie within this low address core.

Initialization

The program initializes by turning off the real time clock (since it will soon destroy the clock vector anyway) and performing a loop which clears the lowest 16,384 words of memory. It then establishes the addresses of all of the ports to be used in hardware registers so that fast register addressing may be used within the monitoring loop. Because the time required to clear the low core in the PDP-11 exceeds 16 milliseconds (the time within which the plasma panel can be expected to have erased) and because the monitoring loop allows no time to check a bulk screen erasure flag anyway, the full screen erase cycle of the panel cannot be performed under terminal control. Thus the user returns to initialization by setting the address of the program into the switch register of the PDP-11 when he wishes to erase the dot memory of the minicomputer. Initialization leads immediately into monitoring without further operator action.

Monitoring Loop

The monitoring loop is quite short and simple and must be so to perform adequately in real time. Once a write or erase request has been detected as described above, the address of the memory word to be altered lies in a hardware register. This address is used in a MOVE instruction to move the selected word to the input of the multiplexor board. The address is then used in another MOVE instruction to place the multiplexor modified word back into the dot array. The loop then continues by checking for the appearance of another request while processing was underway. The resulting instruction times are just under 20 microseconds as required by the plasma panel refresh cycle.

Printout Loop

The contents of the dot memory are moved to a Versatec 200 series printer by the remainder of the software. The only unique portion of this software is caused by the fact that the printer interface expects dot information to be delivered in eight-bit groups and inverted left to right from the order in which they are mapped by the multiplexing hardware. In the printout loop, the printer is initialized, a process which takes several seconds while the electrostatic toner fluid pump is started and stabilizes flow. While the printer is stabilizing, the entire dot map is inverted left to right in eight-bit groups. In this manner, no extra delay is caused by the mapping discrepancy. The 32,768 eight-bit groups comprising the screen image are then moved to the printer with appropriate groups of blanks on each side of each line of the image to create borders on the printed page.

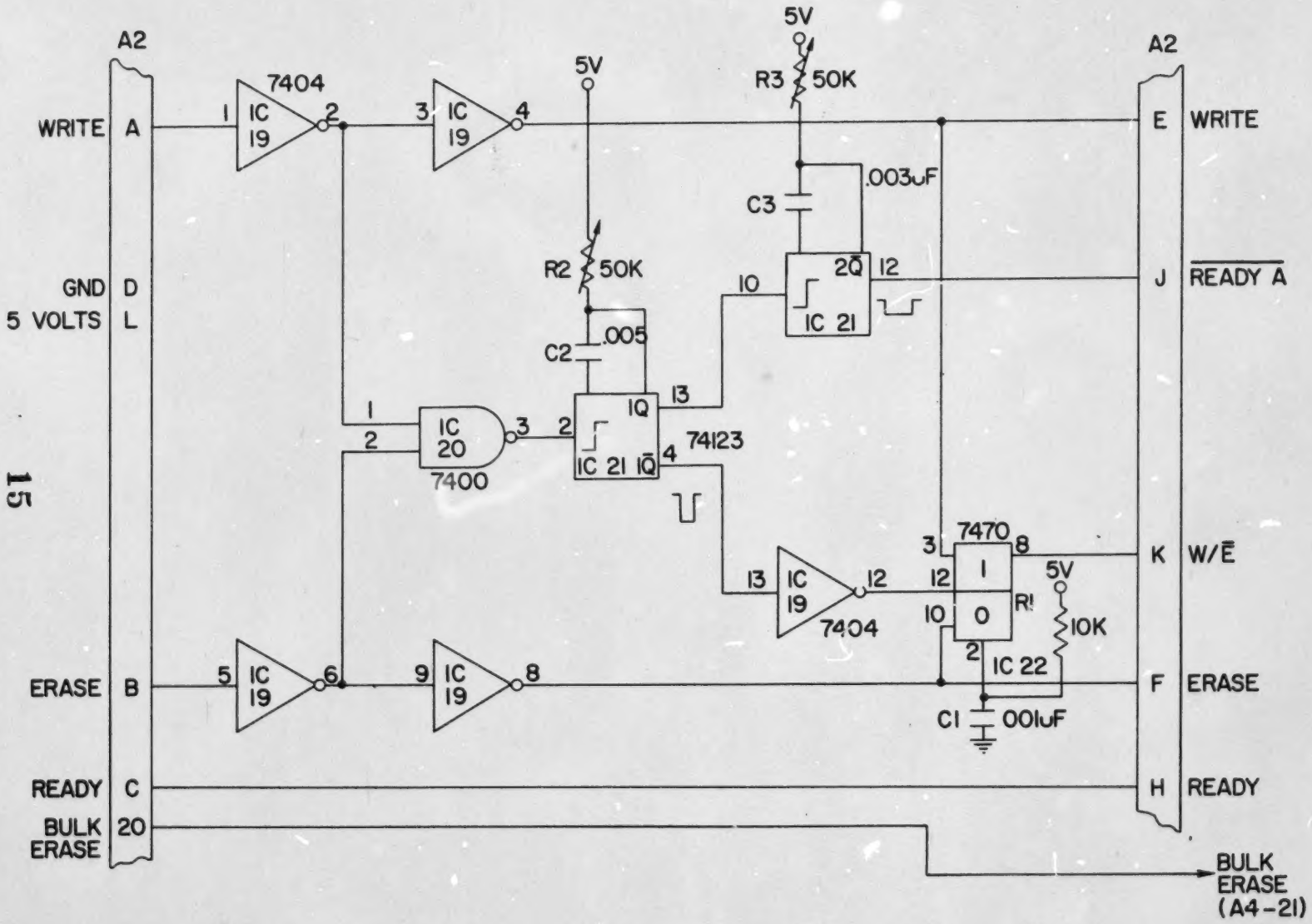
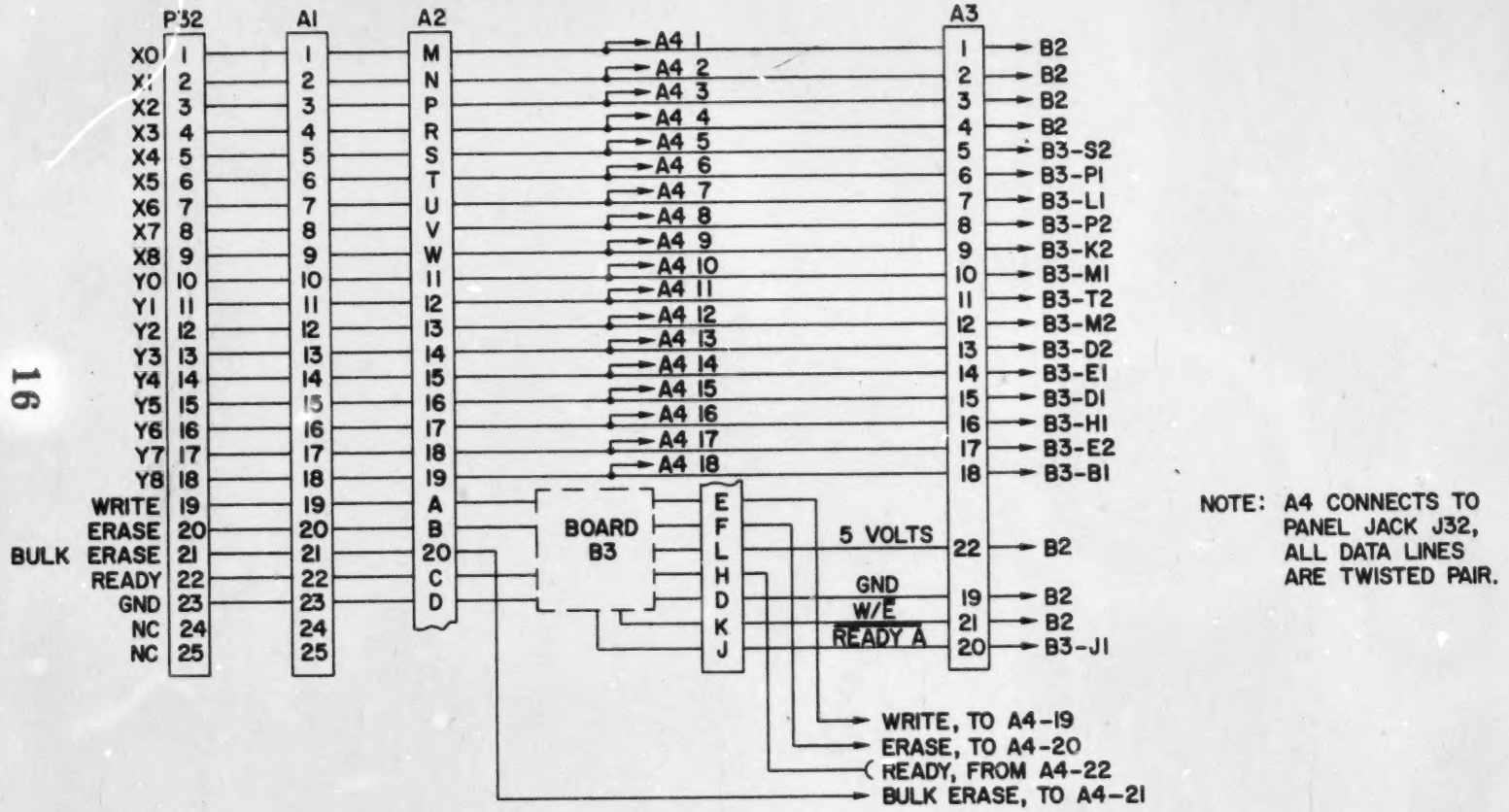


Figure 6. **Hardcopy device control board–B1.**



NOTE: A4 CONNECTS TO PANEL JACK J32, ALL DATA LINES ARE TWISTED PAIR.

Figure 7. **Wiring interconnection diagram.**

Since the Versatec printer prints lines of 560 dots, (560 – 512) / 2 = 24 dots (three eight-bit bytes of zeroes) are added to the beginning and end of each line of 512 dots. This part of the loop needs only to move the data to the printer since it has already been inverted left to right. At this point, the printer is made to eject paper for inter image separation, and the program then waits for requests for additional copies of the same image by the operator. If they are requested, by a depression of the continue switch on the PDP-11 console, they are printed immediately from the already inverted image. Samples of the print produced by the hard copy device are included in Tables 1 and 2.

IV. CONCLUSIONS

The digital approach to a hard copy unit has been found to be both feasible and desirable. Image quality has been found to be much better and precise, and not subject to the variability of quality produced by the optical unit under consideration. The reliability of the Versatec printer has been outstanding, particularly considering that it has never been serviced or even cleaned in three years of operation prior to its use in the hard copy function.

The versatility obtained from the availability of a processor (in this case the PDP-11 processor) to handle the dot data suggests that a hardware version of this simulation should include at least a microprocessor to allow for interface to a number of different printers, and for easy inclusion of special functions such as black on white image inversion and continuous plotting of adjacent images, etc.

With the imminent availability of 16,384 bit random access memory integrated circuits, it should be possible to build a compact and inexpensive version of this simulated digital device if desired. For this reason, it is recommended that no optical copying devices be purchased for use in the Advanced Instructional System in conjunction with plasma screen terminals.

The implications for a cathode ray tube terminal refreshed from a 16 by 16,384 bit digital memory and also providing for connection to a hard copy printer are also quite obvious.

Table 1. **Plasma Macro V06–03 31 Oct 75 12:36**

```
1                       ;THIS IS A DRIVER PROGRAM FOR THE PLASMA PANEL HARD COPY UNIT
2                       ;
3                       ;THE PURPOSE OF THIS DRIVER IS TO MOVE A PARTICULAR BIT BEING
4                       ;WRITTEN OR ERASED BY A PLASMA TERMINAL INTO A 16000 WORD
5                       ;REPRESENTATION OF OF THE VISIBLE DISPLAY
6                       ;THE DISPLAY IS MAPPED INTO THE LOWEST 16K OF THE PDP-11
7                       ;AT THE TIME THAT THE DRIVER IS RUNNING MONITOR CANNOT BE
8                       ;ACTIVE.  ALL INTERRUPTS MUST BE FINISHED BEFORE THE DRIVER
9                       ;IS ACTIVATED, AND THE REAL TIME CLOCK MUST HAVE BEEN
10                      ;DISABLED PRIOR TO THE CLEARING OF THE LOWER 16K OF MEMORY.
11                      ;THE GENERAL PHILOSOPHY OF THIS PROGRAM IS TO
12                      ;  1. BECOME LOADED INTO ONE OF THE HIGHER MEMORY BANKS
13                      ;  2. TURN OFF THE REAL TIME CLOCK
14                      ;  3. CLEAR THE LOWER 16K WORDS OF MEMORY TO ZERO
15                      ;  4. GO INTO A TIGHT LOOP AND WATCH A FLAG BIT IN THE INPUT1
16                      ;     CSR UNTIL IT COMES HIGH INDICATING A REQUEST TO THE PANEL
17                      ;  5. AT THIS TIME THE FOLLOWING SUB STEPS OCCUR:
18                      ;     A)THE WORD ADDRESS ON THE PLASMA SCREEN IS USED AS AN
19                      ;       INDEX INTO THE 16K MAP TO GET THE PROPER 16 BIT GROUP
20                      ;       CORRESPONDING TO THIS PARTICULAR FRAGMENT OF A LINE
21                      ;       SEGMENT OF 16 DOTS (SEE MAP BELOW)
22                      ;     B)THE REMAINING 4 BITS OF ADDRESS ARE BEING FED INTO
23                      ;       THE SPECIAL MULTIPLEXOR BOARD TO SELECT WHICH OF THESE
24                      ;       16 BITS WILL BE CHOSEN TO FOLLOW THE PLASMA READ/WRITE
25                      ;       REQUEST LINE
26                      ;     C)THE ADDRESS INDEX (14 BITS) IS MOVED INTO R2
27                      ;     D)MAP[R2] IS MOVED TO OUTPUT2 PORT
28                      ;     E)16 BIT WORD FROM INPUT2 WHICH NOW CONTAINS THE READ/WRIT
29                      ;       BIT BEING WRITTEN ON THE PANEL IN THE PROPER POSITION
30                      ;       IS MOVED BACK INTO THE PANEL MEMORY MAP
31                      ;     F)THE FLAG BIT IS IMMEDIATLY RETESTED TO SEE IF A SYNCRONO
32                      ;       REREQUEST HAS BEEN MADE WHILE WE WERE BUSY
33                      ;     G)IF SO, WE GO DIRECTLY BACK INTO THE LOOP TO ADD IT,
34                      ;       OTHERWISE WE RETURN TO THE MONITORING LOOP
35                      ;
36                      ;
37                      ;THERE IS NO ESCAPE FROM THIS LOOP, IT MUST BE EXITED BY HALTING
38                      ;THE PDP-11 AND TOGGLING IN A REQUEST TO PRINT THE SCREEN
39                      ;OUTPUT ON THE VERSATEC.
40                      ;
41                      ;WHEN SUCH A TOGGLING IS DONE, THE CONTENTS OF THE MAP ARE PRINT
42                      ;ON THE PRINTER ACCORDING TO THE MAP BELOW, AND THE PROGRAM WAIT
43                      ;FOR A REQUEST FOR MORE COPIES OR FOR A REQUEST FOR A MEMORY
44                      ;CLEAR AND MORE MONITORING.
45                      ;
46                      ;DOS MUST BE RELOADED WHEN FINISHED, AS IT HAS BEEN COMPLETELY
47                      ;DESTROYED BY THIS TIME
48                      ;
49                      ;       E. M. GARDNER           5-OCT-74
50                      ;
51                      .TITLE PLASMA
52      000000'         .PSECT PLASMA
53      177546  RTC=177546              ;LOCATION OF LINE FREQUENCY CLOCK
54      167752  MPXRIN=167752           ;SEND DATA OUT TO THIS PLACE FOR PATCHING
55      167754  MPXROU=167754           ;RECEIVE PATCHED DATA IN AT THIS PLACE
56      167764  ADDRIN=167764           ;RECEIVE 14 BIT ADDR(BITS 1--14) FROM TERM
57                                      ;NOTE: BUILT FROM Y5--Y8 AND X4--X8
```

Table 2. **Plasma Macro V06–03 31 Oct 75 12:36**

```
58          167750 ADDRCS=167753          ;CSR FOR THIS INTERFACE
59
60          177534 VERSAI=177534          ;INPUT BUFFER FROM VERSATEC INTERFACE
61          177532 VERSAO=177532          ;OUTPUT BUFFER TO VERSATEC INTERFACE
62          177530 VERSAC=177533            ;CSR FOR VERSATEC,BIT 15 ON=NOT READY
63
64 00000 005037          CLR     @#RTC              ;TURN OFF THE LINE FREQ CLOCK
           177546
65 00004 005001          CLR     R1                 ;POINT MAP INDX REG TO ADDR 0
66 00006 012702          MOV     #130000,R2         ;PUT LOOP LIMIT IN R2 (16K=LIMIT
           100000
67 00012 005021 CLRMEM:  CLR     (R1)+              ;CLR NEXT CELL OF MAP, BUMP CNTR
68 00014 020102          CMP     R1,R2              ;HAVE WE CLEARED ALL 16K YET?
69 00016 001375          BNE     CLRMEM             ;IF NOT GO BACK AND GET NEXT ONE
70                                                  ;MAP IS ALL ZEROES WHEN WE FINIS
71                                                  ;CORRESPONDING TO BLACK PANEL.
72                                                  ;NOTE: MONITOR IS ALL GONE BYEBY
73
74                                                  ;NOW SETUP FOR MONITORING PANEL
75 00020 012700          MOV     #100000,R0         ;MASK TO TEST FOR PANEL REQUEST
           100000
76 00024 012701          MOV     #ADDRIN,R1         ;INSERT LOC OF PANEL ADDRESS INP
           167764
77                                                  ;PORT INTO R1
78 00030 005002          CLR     R2                 ;R2 USED AS TEMP IN THIS LOOP
79 00032 012703          MOV     #MPXRIN,R3         ;R3 POINTS TO INPUT TO MPXR
           167752
80 00036 012704          MOV     #MPXROU,R4         ;R4 POINTS TO OUTPUT OF MPXR
           167754
81 00042 012705          MOV     #ADDRCS,R5         ;R5 POINTS TO CSR USED TO HOLD
           167750
82 00046 005027          CLR     @ADDRCS            ;CLEAR OUT ADDRCS
           167750
83                                                  ;THE PANEL REQUEST LINE
84
85                                                  ;NOW WE BEGIN THE VERY TIGHT LOO
86                                                  ;THIS LOOP MUST CYCLE IN LESS
87                                                  ;THAN 20 MICROSECS TO FOLLOW THE
88                                                  ;PANEL. THE PANEL CANNOT BE
89                                                  ;SLOWED TO WAIT FOR PDP-11
90
91 00052 011102 MONITR:  MOV     @R1,R2             ;MOVE ADDR + RDY INTO R2
92 00054 100776          BMI     MONITR             ;IF FLAG ON,WAIT
93 00056 011213 MORE:    MOV     @R3,@R3            ;MOVE ARRAY WORD INTO MPXR
94 00060 011412          MOV     @R4,@R2            ;MOVE MPXR OUTPUT INTO ARRAY
95 00062 011102          MOV     @R1,R2             ;BEGIN TO REPEAT LOOP
96 00064 100374          BPL     MORE               ;AND DO MORE IF NEEDED
97 00066 011102          MOV     @R1,R2
98 00070 100372          BPL     MORE
99 00072 000167          JMP     MONITR             ;REPEAT LOOP AT START
           177754
100
101             ;THIS IS THE PRINTOUT LOOP USED TO DUMP CONTENTS OF MEMORY ON TH
102             ;VERSATEC PRINTER
103
104 00076 012700          MOV     #100000,R0             ;MOVE ISR IN ADDR FORM I
           100000
```

Table 2 *(Continued)*

```
105 0132 162704 LOOP16: SUB     #2.,R4                  ;DECREMENT TO NEXT WORD
         000002
106 0136 106164         ROLB    1(R4)                   ;VALID DATA TO CARRY
         000001
107 0112 012705         MOV     #8.,R5                  ;SET UP 8 REPEAT LOOP
         000010
108 0116 106014 LOOP8:  RORB    @R4                             ;WE ARE INVERTIN
109 0120 106164         ROLB    1(R4)                   ;OF THE UPPER AND LOWER
         000001
110 0124 005305         DEC     R5                      ;INDEX INNER LOOP
111 0126 003373         BGT     LOOP8                   ;FINISH INNER LOOP
112 0130 000314         SWAB    (R4)                    ;BYTES ARE SWAPPED AND I
113 0132 005704         TST     R4                      ;OUTER LOOP CHECK
114 0134 001362         BNE     LOOP16                  ;FINISH OUTER LOOP
115
116                 ;HAVE NOW FINISHED REARRANGING ENTIRE MATRIX OF BYTES
117
118 0136 012737         MOV     #175000,@#VERSAD        ;CLEAR PRINTER BUFFER
         175000
         177532
119 0144 012737         MOV     #177000,@#VERSAD        ;CLRS BIT JUST SET
         177000
         177532
120 0152 005737 #AIT0:  TST     @#VERSAC                ;WAIT LOOP FOR PRNTR RDY
         177530
121 0156 100775         BMI     #AIT0                   ;WAIT TIL RDY
122 0160 012737         MOV     #157000,@#VERSAD        ;ISSUE FORM FEED TO EJEC
         167000
         177532
123 0166 012737         MOV     #177000,@#VERSAD        ;CLR BIT JUST SET
         177000
         177532
124 0174 012701 PRINT:  MOV     #130000,R1      ;R1 CONTAINS #BYTES TO PRINT AND
         130000
125                                             ;IS THE TOP OF PAGE BUFFER ALSO
126 0200 162701 LINE:   SUB     #64.,R1         ;POSITION R1 TO HEAD OF NXT LINE
         000100
127
128 0204 005737 #AIT1:  TST     @#VERSAC        ;WAIT LOOP FOR PRINTER
         177530
129 0210 100775         BMI     #AIT1           ;BRANCH BACK TIL NOT RDY GOES LO
130 0212 112737         MOVB    #0,@#VERSAD     ;MOVE "BLANK" FOR LEFT MARGIN
         000000
         177532
131 0220 005737 #AIT2:  TST     @#VERSAC        ;NEED THREE OF THESE FOR EACH BI
         177530
132 0224 100775         BMI     #AIT2           ;SECOND ONE
133 0226 112737         MOVB    #0,@#VERSAD     ;MOVE  IT
         000000
         177532
134 0234 005737 #AIT3:  TST     @#VERSAC
         177530
135 0240 100775         BMI     #AIT3           ;THIRD ONE
136 0242 112737         MOVB    #0,@#VERSAD     ;MOVE IT
         000000
         177532
137
```

Table 2 *(Continued)*

```
138 0250 010102          MOV     R1,R2           ;R1 CONTAINS LINE START ADDR
139 0252 062702          ADD     #64.,R2         ;BUILD LINE END ADDR IN R2
         000100
140 0256 010103          MOV     R1,R3           ;R3 NOW COPY OF LINE START ADDR
141
142 0260 005737 WAIT4:   TST     @#VERSAC        ;WAIT FOR PRINT RDY
         177530
143 0264 100775          BMI     WAIT4           ;AS ABOVE
144 0266 113337          MOVB    (R3)+,@#VERSAD  ;MOVE BYTE TO VERSA, INDX R3 PTR
         177532
145 0272 020302          CMP     R3,R2           ;R3=R2 MEANS THIS LINE DONE
146 0274 001371          BNE     WAIT4           ;IF < THEN NOT DONE 64 BYTES YET
147
148 0276 005737 WAIT5:   TST     @#VERSAC        ;WAIT AGAIN
         177530
149 0302 100775          BMI     WAIT5
150 0304 112737          MOVB    #0,@#VERSAD     ;START LINE ADVANCE(BIT 11)
         000000
         177532
151 0312 112737          MOVB    #0,@#VERSAD     ;REALLY JUST INSERTING RIGHT BDR
         000000
         177532
152 0320 112737          MOVB    #0,@#VERSAD     ;BIT 11 IS REALLY A PULSE
         000000
         177532
153                                              ;LINE AND MUST BE PUSHED LOW, HI
154
155 0326 020127          CMP     R1,#0           ;HAVE WE FINISHED YET, OR MORE L
         000000
156 0332 001401          BEQ     FINISH          ;R1=0 MEANS FINISHED
157 0334 000721          BR      LINE            ;OTHERWISE GO DO NEXT LINE
158
159 0336 005737 FINISH:  TST     @#VERSAC        ;WAIT FOR RDY
         177530
160 0342 100775          BMI     FINISH
161 0344 012737          MOV     #167000,@#VERSAD        ;MOVE ANOTHER FORM FEED
         167000
         177532
162 0352 000637          BR      MONITR
163      000001'         .END
```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